Faculty of Engineering & Technology
Master of Technology (M. Tech)
(W. E. F.: 2023-24)

Document ID: SUTEFETM-01

Name of Faculty	:	Faculty of Engineering & Technology
Name of Program	:	Master of Engineering (M. Tech)
Course Code	:	1MSE05
Course Title	:	Advanced Computer Architecture & Parallel Processing (PE - I)
Type of Course	:	Professional Elective (PE)
Year of Introduction	:	2023-24

Prerequisite	:	Computer Architecture & Digital Logic Design
Course Objective	:	The course objectives of Advanced Computer Architecture and Parallel Processing may vary depending on the institution and the specific curriculum. However, here are some common objectives that are typically associated with this course: Understand the advance Computer Architecture, Exploring Parallel Processing concept, Analyse Performance and Scalability, Design and Optimization of Parallel Processing Algorithms etc.
Course Outcomes	:	At the end of this course, students will be able to:
	CO1	Understand the various techniques to enhance a processors ability to exploit Instruction-level parallelism (ILP), and its challenges.
	CO2	Consider various techniques of instruction-level parallelism, including superscalar execution, branch prediction, and speculation, in design of high- performance processors.
	CO3	Design basic and intermediate RISC pipelines, including the instruction set, data paths, and ways of dealing with pipeline hazards.
	CO4	Verify the performance of computing systems with extended components
	CO5	Develop an understanding of various basic concepts associated with parallel computing environments.

Teaching and Examination Scheme

Teaching Scheme (Contact Hours)			Credits	Examination Marks				
				Theory Marks		Practical Marks		Total Marks
L	T	P	C	SEE	CIA	SEE	CIA	
3	0	2	4	70	30	30	20	150

Legends: ***L****-Lecture;* ***T****–Tutorial/Teacher Guided Theory Practice;* ***P*** *– Practical,* ***C*** *– Credit,* ***SEE*** *– Semester End Examination,* ***CIA*** *- Continuous Internal Assessment (It consists of Assignments/Seminars/Presentations/MCQ Tests, etc.))*

Course Content

Unit No.	Topics	Teaching Hours	Weightage	Mapping with CO
1	**Introduction to Advanced Computer Architecture** Four Decades of Computing, Flynn's Taxonomy of Computer Architecture, SIMD Architecture, MIMD Architecture, Interconnection Networks.	02	04**%**	CO1
2	**Introduction to Parallel Processing** Parallelism in Uniprocessor System, Parallel Computer Structure, Architectural Classification Schemes, Parallel Processing Applications.	05	11**%**	CO2
3	**Parallel Computer Models** Multiprocessors and Multicomputer, Multivector and SIMD Computers, PRAM & VLSI Models, Architectural Development Tracks.	07	16%	CO2
4	**Program and Network Properties** Conditions of Parallelism, Program Partitioning and Scheduling, Program Flow Mechanisms, System Interconnect Architectures.	05	11%	CO5
5	**Principles of Scalable Performance** Performance Metrics and Measures Speedup Performance Laws Scalability Analysis and Approaches.	07	15%	CO4
6	**Processor and Memory Hierarchy** Advanced Processor Technology Superscalar and Vector Processors Memory Hierarchy Technology Virtual Memory Technology.	06	13%	CO4
7	**Bus, Cache & Shared Memory** Bus Systems, Cache Memory Organizations, Shared Memory Organizations, Sequential and Weak Consistency Model.	06	14%	CO5
8	**Pipelining & Superscalar Techniques** Linear Pipeline Processors, Non-Linear Pipeline Processors Instruction Pipeline Design, Arithmetic Pipeline Design Superscalar & Superpipe line Design.	07	16%	CO3

Suggested Distribution of Theory Marks Using Bloom's Taxonomy						
Level	Remembrance	Understanding	Application	Analyse	Evaluate	Create
Weightage	**40**	**20**	**20**	**10**	**-**	**10**

NOTE: This specification table shall be treated as a general guideline for the students and the teachers. The actual distribution of marks in the question paper may vary slightly from above table.

Suggested List of Experiments/Tutorials

Sr. No.	Name of Experiment/Tutorial	Teaching Hours
1	Implement Booth's Algorithm.	2
2	Write the working of 8085 simulator GNUsim8085 and basic architecture of 8085 along with small introduction.	2
3	Write an assembly language code in GNUsim8085 to store numbers in reverse order in memory location.	2
4	Write an assembly language code in GNUsim8085 to implement arithmetic instruction.	2
5	Write an assembly language code in GNUsim8085 to find the factorial of a number.	2
6	Write an assembly language code in GNUsim8085 to implement logical instructions.	2
7	Design ALU using Logisim.	2
8	Implement 16-bit single-cycle MIPS processor in Verilog HDL.	2

Reference Books

Sr. No.	Name of Reference Books
1	Kai Hwang, Faye A. Briggs, "Computer Architecture and Parallel Processing", Tata McGraw Hill.
2	Hesham El-Rewini,Mostafa Abd-El-Barr "Advanced Computer Architecture and Parallel Processing", Wiley
3	Introduction to Parallel Computing, Ananth Grama, Anshul Gupta, George Karypis, Vipin Kumar, By Pearson Publication
4	Introduction to Parallel Processing, M. SasiKumar, Dinesh Shikhare, P.Raviprakash By PHI Publication Steven Brawer,
5	Introduction To Parallel Programming, Academic Pr
6	M.Sasikumar, Dinesh Shikhare and P. Ravi Prakash, Introduction to Parallel Processing, Prentice Hall of India.
7	V. Rajaraman and C. Siva Ram Murthy, Parallel Computers – Architecture and Programming, Prentice Hall of India.